Attorney Docket: 0325.00420

IN RE APPLICATION OF: Navaz Lulla et al.

SERIAL NO.: 09/689,532

RESPONSE TRANSMITTAL AND EXTENSION OF TIME REQUEST (IF REQUIRED)

TITLE: CIRCUIT FOR GENERATING SILICON ID FOR PLDS

FILED: October 12, 2000

EXAMINER: Whitmore, S.

ART UNIT: 2812

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COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

FEE CALCULATION FOR ENCLOSED AND EXTENSION REQUEST (IF ANY)

	Claims Remaining	Highest No. Previous	Extra Rate	Additional Fee
Total Claims	26 minus	26 =	0 x $ 18.00	$ 0.00
Independent Claims	3 minus	3 =	0 x $ 86.00	$ 0.00
Multiple Dependent Claim First Added			+ $290.00	$ 0.00

TOTAL IF NOT SMALL ENTITY . . $0.00

[ ] SMALL ENTITY STATUS - If applicable, divide by 2 . . . . . $0.00
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[ ] Applicant also requests a ____ month extension of time for response to the outstanding Office Action. The fee is $0.00

[X] Fee set forth for Appeal Brief $330.00

TOTAL FEE $330.00

The Commissioner is hereby authorized to charge any overpayment or underpayment of the above fee associated with this Communication to Deposit Account No. 50-0541. A duplicate copy of this sheet is attached.

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I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 22, 2004.

By: _____
Jan M. Dunbar

Our Docket No.: 0325.00420

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Applicant	Navaz Lulla et al.	
Application No.:	09/689,532	Examiner: Whitmore, S.
Filed:	October 12, 2000	Art Group: 2812
For:	CIRCUIT FOR GENERATING SILICON ID FOR PLDS	

CERTIFICATE OF MAILING

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop Appeal Brief Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 22, 2004.

By: Jan M Dunbar
Jan M. Dunbar

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellants submit the following Appeal Brief pursuant to 37 C.F.R. §41.37 for consideration by the Board of Patent Appeals and Interferences. Appellants also submit herewith a PTO-2038 Form in the amount of $330.00 to cover the cost of filing the opening brief as required by 37 C.F.R. §42.20(b)(2). Please charge any additional fees or credit any overpayment to our Deposit Account Number 50-0541.

TABLE OF CONTENTS

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[1] U.S. Patent No. 5,467,304; hereinafter Uchida.

[2] U.S. Patent No. 6,308,311; hereinafter Carmichael.

[3] U.S. Patent No. 6,311,246; hereinafter Wegner.

I. REAL PARTY IN INTEREST

The real party in interest is the Assignee, Cypress Semiconductor Corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Appellants, Appellants' legal representative, or Assignee which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-26 are pending and remain rejected. The Appellants hereby appeal the rejection of claims 1-26.

IV. STATUS OF AMENDMENTS

Appellants are appealing a final Office Action issued by the Examiner on March 26, 2004. On May 26, 2004, Appellants filed an Amendment After Final amending claims 1, 3, 20 and 21. The Amendment After Final filed May 26, 2004 was not entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In a first embodiment, the present invention concerns an apparatus comprising a logic circuit (110 in FIG. 3 or 250 in FIG. 5) comprising (i) one or more first inputs (114 in FIG. 3) each connected to a respective one of one or more pins (92 in FIG. 3 and page 7, lines 13-14), (ii) one or more second inputs (112 in FIG. 3) each connected to a respective one of one or more bond options

(page 7, lines 11-13), (iii) one or more third inputs (116 in FIG. 3) each connected to a respective one of one or more metal options (302, 304 and 310a-o in FIG. 6 and page 7, line 16) and (iv) an output (118 in FIG. 3) configured to present a plurality of identification codes (IDCD in FIG. 3 and page 7, lines 16-17), wherein said logic circuit is configured to generate said plurality of identification (ID) codes in response to a logical combination of (i) one or more voltage levels on said one or more first inputs (page 6, lines 9-15), (ii) a state of said one or more bond options and (iii) a state of said one or more metal options (page 7, lines 19-21 and page 25, lines 3-5) and a package (90 in FIG. 3 and page 9, line 12 - page 10, line 10) comprising said one or more pins, wherein said one or more pins are dedicated to providing said one or more voltage levels to respective ones of said one or more first inputs (page 8, lines 3-7).

In a second embodiment, the presently claimed invention concerns a method of providing a plurality of identification codes (IDCD in FIG. 3) for a single die and package combination comprising the steps of (A) dedicating (i) one or more pins (92) of the package (90), (ii) one or more bond options and (iii) one or more metal options (302, 304 and 310a-o in FIG. 6) to generating a plurality of identification codes, (B) generating the plurality of identification codes in response to a logical combination of (i) voltage levels on the one or more pins (pin 92 connected to input 114 in FIG. 3 and page 6, lines 9-15), (ii) a state of the one or more bond options and (iii) a state of the one or more metal options and (C) providing an indication of the voltage levels to be applied to each of the one or more pins (page 8, lines 5-7).

In a third embodiment, the present invention concerns an apparatus comprising (a) means for generating a plurality of identification codes (110 in FIG. 3) in response to a logical combination of (i) one or more voltage levels asserted at one or more first inputs (114 in FIG. 3 and

page 6, lines 9-15), (ii) a state of one or more bond options connected to one or more second inputs (112 in FIG. 3) and (iii) a state of one or more metal options connected to one or more third inputs (116 in FIG. 3) and (b) means for packaging (90 in FIG. 3 and page 9, line 12 through page 10, line 10) the generating means comprising one or more pins (92 in FIG. 3) dedicated to providing the one or more voltage levels to respective ones of the one or more first inputs.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The rejection of claims 1, 3, 4, 10, 12, 16, 17, 20-22 and 24-26 under 35 U.S.C. §102(b) as being anticipated by Uchida et al.[4] (hereafter Uchida).

The rejection of claims 2 and 5-9 under 35 U.S.C. §103(a) as being obvious over Uchida in view of "IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990" (hereinafter IEEE Std 1149.1-1990).

The rejection of claims 11, 13 and 14 under 35 U.S.C. §103(a) as being obvious over Uchida in view of Carmichael et al.[5] (hereinafter Carmichael).

The rejection of claim 15 and 23 under 35 U.S.C. §103(a) as being obvious over Uchida in view of Carmichael and further in view of Wegner et al.[6] (hereinafter Wegner).

The rejection of claims 18 and 19 under 35 U.S.C. §103(a) as being obvious over Uchida in view of IBM TDB Publication, "Using a Portion of the Boundary Register as the

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[4] U.S. Patent No. 5,467,304.

[5] U.S. Patent No. 6,308,311.

[6] U.S. Patent No. 6,311,246.

Identification Register" (hereinafter IBM) and further in view of "IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990" (hereinafter IEEE Std 1149.1-1990).

VII. ARGUMENTS

A. Rejections under 35 U.S.C. § 102

As set forth on page 2 of the final Office Action[7], claims 1, 3, 4, 10, 12, 16, 17, 20-22 and 24-26 under 35 U.S.C. §102(b) as being anticipated by Uchida et al.[8]

The Federal Circuit has stated that "[t]o anticipate, *every element and limitation* of the claimed invention must be found in a single prior art reference, *arranged as in the claim.*"[9] The Federal circuit has added that the anticipation determination is viewed from one of ordinary skill in the art: "There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention."[10] Furthermore, "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference."[11] As explained herein below, because Uchida does not disclose or suggest a logic circuit configured to generate a plurality of identification codes in response to **a logical combination of (i) one or more voltage levels on one or more pins, (ii) a state of one or more bond options AND (iii) a state of one or more metal options** as presently

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[7] Dated March 26, 2004.

[8] U.S. Patent No. 5,467,304; hereinafter Uchida.

[9] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991) (Emphasis added by Appellants).

[10] *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

[11] *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, USPQ2d 1051, 1053 (Fed Circ. 1987).

claimed, Uchida does not anticipate the presently claimed invention. As such, the rejection should be reversed.

1. Claims 1, 3, 4, 10, 12, 16, 17, 20-22 and 24-26 are patentable over Uchida et al.[12]

The presently pending claim 1 provides an apparatus comprising (A) a logic circuit comprising (i) one or more first inputs each connected to a respective one of one or more pins, (ii) one or more second inputs each connected to a respective one of one or more bond options, (iii) one or more third inputs each connected to a respective one of one or more metal options and (iv) an output configured to present a plurality of identification codes, wherein said logic circuit is configured to generate said plurality of identification (ID) codes in response to a logical combination of (i) one or more voltage levels on said one or more first inputs , (ii) a state of said one or more bond options and (iii) a state of said one or more metal options and (B) a package comprising said one or more pins, wherein said one or more pins are dedicated to providing said one or more voltage levels to respective ones of said one or more first inputs. Claims 16 and 20 recite similar limitations. Claims 3, 4, 10, 12, 17, 21, 22 and 24-26 depend, directly or indirectly, from either claim 1, claim 16 or claim 20.

Uchida is directed to a semiconductor integrated circuit.[13] Uchida describes selecting an identification code for a device via the diffusion process and bond optioning bonding pads to a

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[12] U.S. Patent No. 5,467,304; hereinafter Uchida.

[13] Title of Uchida.

GND pin during assembly.[14] Since Uchida determines an identification code using only the diffusion process and bond options, it follows that Uchida does not disclose or suggest a logic circuit configured to generate a plurality of identification codes in response to **a logical combination of (i) one or more voltage levels on one or more first inputs, (ii) a state of one or more bond options AND (iii) a state of one or more metal options**, as presently claimed. Therefore, Uchida does not disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. As such, claims 1, 3, 4, 10, 12, 16, 17, 20-22 and 24-26 are fully patentable over Uchida and the rejection should be reversed.

Furthermore, assuming, *arguendo*, that (i) elements 6 and 7 of Uchida are similar to the presently claimed bond options, (ii) GND in element 4, VCC in element 5, and elements 31 and 32 of Uchida are similar to the presently claimed metal options and (iii) elements 9 and 10 of Uchida are similar to the pins for receiving the one or more voltage levels as presently claimed,[15] Uchida does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. In particular, the Examiner presents no evidence or convincing line of reasoning why one of ordinary skill in the field of the present invention would consider elements 9 and 10 of Uchida as having no differences from the presently claimed one or more voltage levels on the one or more first inputs which are logically combined with (i) the state of one or more bond options AND (iii) the state of one or more metal options to generate the ID codes.[16]

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[14] See column 3, line 58 through column 4, line 5 and column 6, lines 14-33 of Uchida.

[15] As suggested on page 2, section 4 of the Office Action and for which Appellants' representative does not necessarily agree.

[16] See page 2, section 4, pages 3-5, sections 9-11 of the final Office Action dated March 26, 2004.

Specifically, the elements 9 and 10 of Uchida are described as a shift clock input pad and a ID code setting pad, respectively.[17] The signal presented at the element 10 of Uchida loads an ID code into a shift register formed by elements 4 and 5 of Uchida.[18] The signal presented to the element 9 of Uchida serializes the ID code by shifting the code through the shift register formed by elements 4 and 5 of Uchida.[19] In particular, Uchida states:

> Here, when the signal for the ID setting pad 10 is turned into high level, the multiplexers 41 to 43 output the levels of A-terminals to the O-terminal. Next, when the shift clock to the shift clock pad 9 is turned into high level, high level is held in the F/F 51, low level is held in the F/F 52, high level held in the F/F 53, low level is held the F/F 54, and then high level is output from the ID code output pad 8.
>
> After turning the signal for the ID code setting pad 10 into low level, when shift clock for three clocks is input to the shift clock pad 9, low level, low level and high level are output in order from the ID code output pad 8.
>
> At this time, by setting so that the ID code is output sequentially in an order from the least significant bit (LSB) to the most significant bit (MSB), the ID code "1001" can be output as the ID code for the kind C.
>
> Similarly, for remaining kinds A, B and D, the ID codes respectively corresponding thereto can be output depending upon whether the bonding option pads 6 and 7 are bonded to the GND pins.(column 6, line 51 through column 7, line 5 of Uchida).

One skilled in the in the field of the invention would not consider (i) a voltage level at the pad 10 of Uchida which loads an ID code predetermined by the diffusion process and bond options into the shift register formed by elements 4 and 5 of Uchida and (ii) a voltage level at the shift clock input pad 9 of Uchida which shifts the predetermined ID code through the shift register formed by

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[17] See column 5, lines 23-36 of Uchida.

[18] See FIG. 2 and column 6, lines 53-56 of Uchida.

[19] See FIGS. 2, 4, 8 and 9 and column 6, line 51 through column 7, line 5 of Uchida.

elements 4 and 5 of Uchida to be the same as the presently claimed one or more voltage levels on one or more first inputs which are **logically combined** with the state of one or more bond options and the state of one or more metal options **to generate** a plurality of identification codes, as presently claimed. The Examiner appears to confuse generating the ID codes, as presently claimed, with presenting (or shifting out) already generated ID codes as performed by the elements 9 and 10 of Uchida.

Furthermore, Uchida does not disclose or suggest generating an ID code by **logically combining** (i) one or more voltage levels on one or more first inputs, (ii) a state of one or more bond options **AND** (iii) a state of one or more metal options, as presently claimed. Specifically, the ID codes generated by the circuit of Uchida are determined **ONLY** by the bond option pads 6 and 7 and logic levels set in the diffusion process. In particular, Uchida states:

> For instance, **in the diffusion process, the ID code becomes "10XX**[.]" In this ID code, **X is "0" or "1" which is determined whether the bonding option pads 6 and 7 are bonded to the GND pins or not.**[20]

Uchida is silent regarding logically combining voltage levels at pins 9 and 10 with a state of the bond option pads 6 and 7 and the logic levels set in the diffusions process to generate ID codes. With respect to generating the ID codes, Uchida further states:

> When the bonding option pads 6 and 7 are both bonded to the GND pins (step S4 of FIG. 3), the IC chip becomes a kind A (step S5 of FIG. 3) and then the ID code becomes "1000".
> On the other hand, when only bonding option pad 6 is bonded to the GND pin (step S6 of FIG. 3), IC chip becomes a kind B (step S7 of FIG. 3) and then the ID code becomes "1010".

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[20] Column 6, lines 14-17 of Uchida, emphasis added.

> Also, when only bonding option pad 7 is bonded to the GND pin (step S8 of FIG. 3), IC chip becomes a kind C (step S9 of FIG. 3) and then the ID code becomes "1001".
> When the bonding option pads 6 and 7 are both not bonded to the GND pins (step S10 of FIG. 3), IC chip becomes a kind D (step S11 of FIG. 3) and then the ID code becomes "1011" (column 6, lines 18-33 of Uchida).

Since each bit of the ID codes of Uchida is directly determined by a respective bond option or diffusion, one skilled in the art would not view the circuit of Uchida as generating an ID code by **logically combining** (i) one or more voltage levels on one or more first inputs, (ii) a state of one or more bond options **AND** (iii) a state of one or more metal options, as presently claimed.

The specification provides, for example on pages 14-24, numerous examples of identification codes generated by **logically combining** (i) one or more voltage levels on one or more first inputs, (ii) a state of one or more bond options **AND** (iii) a state of one or more metal options, as presently claimed. The Examiner presents no evidence or convincing line of reasoning why one of ordinary skill in the field of the present invention would consider the circuit of Uchida as having no differences from the logic circuit configured to generate a plurality of ID codes in response to a **logical combination of** (i) one or more voltage levels on one or more first inputs, (ii) a state of one or more bond options **AND** (iii) a state of one or more metal options, as presently claimed. Therefore, Uchida does not disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. As such, claims 1, 3, 4, 10, 12, 16, 17, 20-22 and 24-26 are fully patentable over Uchida and the rejection should be reversed.

Furthermore, the conclusory statement on page 4, lines 22-26 of the final Office Action[21] that:

> . . . the logical combination of (i) through (iii) is comprised of the combination of elements 6-7 (bonding options), one or more voltage levels (elements 9 or 10); and a state of one or more metal options (elements 31, 32 or GRD [sic; GND] in element 4 or Vcc in element 5).

does not address (i) what the alleged combination is or (ii) why the alleged combination of signals would be considered by one of ordinary skill in the field of the present invention as a logical combination, as presently claimed.[22] The Examiner appears to be trying to shift the burden to the Appellant to prove a negative (i.e., that the signals are not logically combined) rather than meeting the Office's burden to factually establish that one skilled in the art would view the disclosure of Uchida as having no differences from the presently claimed invention.

Furthermore, the interpretation of the elements 31 and 32 of Uchida as being the same as the presently claimed metal options is not technically correct. Specifically, Uchida states:

> In FIG. 2, the **bonding judgement portion 3** comprises **P-channel transistors 31 and 32**. P-channel **transistors 31 and 32** are set at small current capacity so that they may **serve as pull-up resistance for the signal lines 101 and 102 from the bonding option pads 6 and 7** to the function circuit portion and the ID setting portion by connecting the gates thereof to the GND level.[23]

Rather than being separate options from the bond options, as presently claimed, the elements 31 and 32 of Uchida are an integral part of the bond option capability of elements 6 and 7. In particular,

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[21] Dated March 26, 2004

[22] See page 4, lines 22-26 of the final Office Action dated March 26, 2004.

[23] Column 5, lines 44-50 of Uchida, emphasis added.

elements 31 and 32 allow the signal lines 101 and 102, respectively, to become high when the bond option pads 6 and 7 are not bonded to the GND pin.[24]

Furthermore, the Examiner on page 3, last line, of the final Office Action associates elements 6 and 7 with the presently claimed one or more first inputs. However, in contradiction to the Examiner's position on page 3, on page 4, lines 5-6 of the final Office Action, the Examiner associates elements 6 and 7 with the presently claimed bonding options. Clearly, if elements 6 and 7 correspond to the presently claimed one or more first inputs (or pins), it follows that elements 6 and 7 cannot be the one or more bonding options. Alternatively, if elements 6 and 7 correspond to the presently claimed one or more bonding options, it follows that elements 6 and 7 cannot correspond also to the presently claimed one or more first inputs (or pins) .

Furthermore, one of ordinary skill in the field of the invention would not consider the presently claimed bond options to be the same as the presently claimed one or more voltage levels presented at the presently claimed one or more first inputs (or pins). Specifically, bond options are set during packaging and are not accessible afterward unless the package is re-opened. In contrast, one of skill in the field of the invention would recognize that the one or more first inputs (or pins), as presently claimed, are accessible after packaging and, therefore, are not the same as bond options. Therefore, the Examiner has failed to meet the Office's burden to factually establish a *prima facie* conclusion of anticipation. As such, claims 1, 3, 4, 10, 12, 16, 17, 20-22 and 24-26 are fully patentable over the cited reference and the rejection should be reversed.

For the reasons presented above, Uchida does not disclose or suggest a logic circuit configured to generate a plurality of identification codes in response to **a logical combination of (i)**

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[24] See column 6, lines 46-49 of Uchida.

one or more voltage levels on one or more first inputs, (ii) a state of one or more bond options AND (iii) a state of one or more metal options, as presently claimed. Therefore, Uchida does not disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. As such, claims 1, 3, 4, 10, 12, 16, 17, 20-22 and 24-26 are fully patentable over Uchida and the rejection should be reversed.

B. Rejections under 35 U.S.C. § 103

As set forth on pages 6-10 of the final Office Action,[25] claims 2, 5-9, 11, 13-15, 18, 19 and 23 are rejected under 35 U.S.C. § 103(a).[26]

Three criteria are required to establish a prima facie case of obviousness. The Examiner must show that (1) there is some suggestion or motivation, either in the references or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the references, (2) there is a reasonable expectation of success, and (3) the prior art reference (or combination of references) teaches or suggests *all of the claim limitations*.[27]

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[25] Dated March 26, 2004

[26] Claims 2 and 5-9 are rejected under 35 U.S.C. § 103(a) as being obvious over Uchida in view of "IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990" (hereinafter IEEE Std 1149.1-1990), claims 11, 13 and 14 are rejected under 35 U.S.C. §103(a) as being obvious over Uchida in view of Carmichael et al. (U.S. Patent No. 6,308,311; hereinafter Carmichael), claims 15 and 23 are rejected under 35 U.S.C. §103(a) as being obvious over Uchida in view of Carmichael and further in view of Wegner et al. (U.S. Patent No. 6,311,246; hereinafter Wegner), and claims 18 and 19 are rejected under 35 U.S.C. §103(a) as being obvious over Uchida in view of IBM TDB Publication, "Using a portion of the boundary register as the identification register" (hereinafter IBM)and further in view of "IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990" (hereinafter IEEE Std 1149.1-1990).

[27] Manual of Patent Examining Procedure (MPEP), Eighth Edition, Revision 2, May 2004, §2142. (emphasis added).

The Federal Circuit has held that both the suggestion to modify or combine the references and the reasonable expectation of success must be found in the prior art itself, not merely in Appellant's disclosure.[28] Furthermore, the Board has held that the claimed invention is obvious only if either the references expressly or implicitly suggest the claimed invention, or a convincing line of reasoning is presented by the examiner as to why an artisan would have found the claimed invention to be obvious in light of the teachings of the cited references.[29]

1. Claims 2 and 5-9 are patentable over Uchida in view of IEEE Std 1149.1-1990.

Claims 2 and 5-9 depend, either directly or indirectly, from claim 1 and, therefore, include all the limitations of claim 1. Consequently, the arguments present above in support of claim 1 are incorporated herein by reference in support of claims 2 and 5-9.

For the reasons presented above, Uchida does not teach or suggest a logic circuit configured to generate a plurality of identification codes in response to **a logical combination of (i) one or more voltage levels on one or more first inputs (or pins), (ii) a state of one or more bond options AND (iii) a state of one or more metal options**, as presently claimed. The Examiner presented no evidence or convincing line of reasoning to support a position that IEEE Std 1149.1-1990 teaches or suggests a logic circuit configured to generate a plurality of identification codes in response to **a logical combination of (i) one or more voltage levels on one or more first inputs (or pins), (ii) a state of one or more bond options AND (iii) a state of one or more metal options,**

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[28] See In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438, 1442 (Fed. Cir. 1991).

[29] See Ex Parte Clapp, 227 U.S.P.Q. 972, 973 (Bd. Pat. App. & Inter. 1985).

as presently claimed. Because the cited references fail to teach or suggest each and every limitation of the presently pending claims, the Examiner failed to meet the Office's burden of factually establishing a *prima facie* case of obviousness. As such, claims 2 and 5-9 are fully patentable over the cited references and the rejections should be reversed.

2. Claims 11, 13 and 14 are patentable over Uchida in view of Carmichael.

Claims 11, 13 and 14 depend, either directly or indirectly, from claim 1 and, therefore, include all the limitations of claim 1. Consequently, the arguments present above in support of claim 1 are incorporated herein by reference in support of claims 11, 13 and 14. Claim 11 further recites wherein said metal options are set to indicate an operating voltage of said apparatus.

For the reasons presented above, Uchida does not teach or suggest a logic circuit configured to generate a plurality of identification codes in response to **a logical combination of (i) one or more voltage levels on one or more first inputs (or pins), (ii) a state of one or more bond options AND (iii) a state of one or more metal options**, as presently claimed. The Examiner presented no evidence or convincing line of reasoning to support a position that Carmichael teaches or suggests a logic circuit configured to generate a plurality of identification codes in response to **a logical combination of (i) one or more voltage levels on one or more first inputs (or pins), (ii) a state of one or more bond options AND (iii) a state of one or more metal options**, as presently claimed.

Furthermore, the Examiner admits that Uchida does not specifically teach wherein said metal options are set to indicate an operating voltage of said apparatus.[30] Carmichael does not cure the deficiencies of Uchida. Specifically, the text of Carmichael cited by the Examiner[31] reads:

> Microcontroller 34 writes to register 74 a control bit having a logic value indicative of whether target FPGA 10 is a 3.3 volt device or a 2.5 volt device. For example, if the target FPGA 10 is a 3.3 volt device, microcontroller 34 writes a logic zero to register 72 and, conversely, if target FPGA 10 is a 2.5 volt device, microcontroller 34 writes a logic one to register 74.[32]

Contrary to the Examiner's statement,[33] nowhere in the above text does Carmichael expressly mention either (i) metal options are set to indicate an operating voltage of the apparatus, as recited in claim 11 or (ii) pins are labeled as either a first or second supply voltage based on characteristics of the apparatus as recited in claims 13 and 14. Because the cited references fail to teach or suggest each and every limitation of the presently pending claims, the Examiner failed to meet the Office's burden of factually establishing a *prima facie* case of obviousness. As such, claims 11, 13 and 14 are fully patentable over the cited references and the rejections should be reversed.

Furthermore, because the Examiner fails to explain the specific understanding or principle within the knowledge of a person skilled in the field of the invention that would motivate one, with no knowledge of the presently claimed invention, to have selected Carmichael for combination with Uchida, the Examiner failed to meet the Office's burden to factually establish a

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[30] See page 8, lines 8-9 of the final Office Action dated March 26, 2004.

[31] See page 8, lines 10-11 and 21-22 in the final Office Action dated March 26, 2004.

[32] Column 12, line 67 - column 13, line 4 of Carmichael.

[33] See page 8, lines 10-11 and 21-22 in the final Office Action dated March 26, 2004.

prima facie case of obviousness.[34] As such, the presently claimed invention is fully patentable over the cited references and the rejection should be reversed.

3. Claims 15 and 23 are patentable over Uchida in view of Carmichael and further in view of Wegner et al.[35]

Claims 15 and 23 depend, either directly or indirectly, from claim 1 and, therefore, include all the limitations of claim 1. Consequently, the arguments present above in support of claim 1 are incorporated herein by reference in support of claims 15 and 23.

For the reasons presented above, Uchida does not teach or suggest a logic circuit configured to generate a plurality of identification codes in response to **a logical combination of (i) one or more voltage levels on one or more first inputs (or pins), (ii) a state of one or more bond options AND (iii) a state of one or more metal options**, as presently claimed. The Examiner presented no evidence or convincing line of reasoning to support a position that either Carmichael or Wegner teaches or suggests a logic circuit configured to generate a plurality of identification codes in response to **a logical combination of (i) one or more voltage levels on one or more first inputs (or pins), (ii) a state of one or more bond options AND (iii) a state of one or more metal options**, as presently claimed. Because the cited references fail to teach or suggest each and every limitation of the presently pending claims, the Examiner failed to meet the Office's burden of factually establishing a *prima facie* case of obviousness. As such, claims 15 and 23 are fully patentable over the cited references and the rejections should be reversed.

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[34] MPEP §2142.

[35] U.S. Patent No. 6,311,246; hereinafter Wegner.

Furthermore, because the Examiner fails to explain the specific understanding or principle within the knowledge of a person skilled in the field of the invention that would motivate one, with no knowledge of the presently claimed invention, to have selected Carmichael and Wegner for combination with Uchida, the Examiner failed to meet the Office's burden to factually establish a *prima facie* case of obviousness.[36] As such, the presently claimed invention is fully patentable over the cited references and the rejection should be reversed.

4. Claims 18 and 19 are patentable over Uchida in view of IBM TDB Publication, "Using a portion of the boundary register as the identification register" (hereinafter IBM) and further in view of "IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990" (hereinafter IEEE Std 1149.1-1990).

Claims 18 and 19 depend, either directly or indirectly, from claim 16 and, therefore, include all the limitations of claim 16. Consequently, the arguments present above in support of claims 1, 3, 4, 10, 12, 16, 17, 20-22 and 24-26 are incorporated herein by reference in support of claims 18 and 19.

For the reasons presented above, Uchida does not teach or suggest a logic circuit configured to generate a plurality of identification codes in response to **a logical combination of (i) one or more voltage levels on one or more first inputs (or pins), (ii) a state of one or more bond options AND (iii) a state of one or more metal options**, as presently claimed. The Examiner presented no evidence or convincing line of reasoning to support a position that either IBM or IEEE 1149.1-1990 teaches or suggests a logic circuit configured to generate a plurality of identification codes in response to **a logical combination of (i) one or more voltage levels on one or more first**

[36] M.P.E.P. § 2142.

inputs (or pins), (ii) a state of one or more bond options AND (iii) a state of one or more metal options, as presently claimed. Because the cited references fail to teach or suggest each and every limitation of the presently pending claims, the Examiner failed to meet the Office's burden of factually establishing a *prima facie* case of obviousness.[37] As such, claims 18 and 19 are fully patentable over the cited references and the rejections should be reversed.

[37] M.P.E.P. § 2142.

C. CONCLUSION

None of the cited references teach or suggest either (i) a logic circuit configured to generate a plurality of identification codes in response to **a logical combination of (i) one or more voltage levels on one or more first inputs (or pins), (ii) a state of one or more bond options AND (iii) a state of one or more metal options** or (ii) generating a plurality of identification codes in response to **a logical combination of (i) one or more voltage levels on one or more first inputs (or pins), (ii) a state of one or more bond options AND (iii) a state of one or more metal options,** as recited in the independent claims 1, 16 and 20. Hence, the Examiner has clearly erred with respect to the patentability of the claimed invention. It is respectfully requested that the Board overturn the Examiner's rejection of all pending claims, and hold that the claims are not rendered obvious by the cited references.

Respectfully submitted,

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IX. CLAIM APPENDIX

The claims of the present application which are involved in this appeal are as follows:

1. An apparatus comprising:

a logic circuit comprising (i) one or more first inputs each connected to a respective one of one or more pins, (ii) one or more second inputs each connected to a respective one of one or more bond options, (iii) one or more third inputs each connected to a respective one of one or more metal options and (iv) an output configured to present a plurality of identification codes, wherein said logic circuit is configured to generate said plurality of identification (ID) codes in response to a logical combination of (i) one or more voltage levels on said one or more first inputs, (ii) a state of said one or more bond options and (iii) a state of said one or more metal options; and

a package comprising said one or more pins, wherein said one or more pins are dedicated to providing said one or more voltage levels to respective ones of said one or more first inputs.

2. The apparatus according to claim 1, wherein said ID codes comprise a silicon ID of an electronic part.

3. The apparatus according to claim 1, wherein said logic circuit is further configured to generate said plurality of ID codes having a number of bits less than a total number of said metal options, said bond options, and said pins.

4. The apparatus according to claim 1, wherein said one or more pins are

connectable to either a voltage supply power or a voltage supply ground according to markings on said package.

5. The apparatus according to claim 1, wherein each of said plurality of ID codes comprises a part number for said apparatus.

6. The apparatus according to claim 5, wherein said part number is combined with other identification codes.

7. The apparatus according to claim 6, wherein said other ID codes comprise one or more codes selected from the group consisting of a version number and a manufacturing number.

8. The apparatus according to claim 1, further comprising a register configured to capture said ID codes from said output of said logic circuit in response to an identification request.

9. The apparatus according to claim 8, wherein said register comprises a JTAG ID code register.

10. The apparatus according to claim 1, wherein said apparatus comprises a programmable logic device (PLD).

11. The apparatus according to claim 1, wherein said metal options are set to

indicate an operating voltage of said apparatus.

12. The apparatus according to claim 1, wherein said bond options are set based on a style of said package of said apparatus.

13. The apparatus according to claim 1, wherein said one or more pins are labeled as either a first or a second supply voltage.

14. The apparatus according to claim 13, wherein said one or more pins are labeled as either said first or said second supply voltage based on characteristics of said apparatus.

15. The apparatus according to claim 14, wherein said characteristics comprise one or more characteristics selected from the group consisting of volatility, price, package, metal options, operating voltage, internal structure, part category and density.

16. A method of providing a plurality of identification codes for a single die and package combination comprising the steps of:

(A) dedicating (i) one or more pins of said package, (ii) one or more bond options and (iii) one or more metal options to generating a plurality of identification codes;

(B) generating said plurality of identification codes in response to a logical combination of (i) voltage levels on said one or more pins, (ii) a state of said one or more bond options and (iii) a state of said one or more metal options; and

(C) providing an indication of said voltage levels to be applied to each of said one or more pins.

17. The method according to claim 16, wherein the step (B) further comprises the steps of:

determining said voltage levels on said one or more pins;

determining said state of said one or more metal options;

determining said state of said one or more bond options; and

logically combining a result of each determining step.

18. The method according to claim 16, further comprising the step of:

presenting a generated identification code in response to an identification request.

19. The method according to claim 18, wherein said identification request comprises a JTAG ID code instruction.

20. An apparatus comprising:

means for generating a plurality of identification codes in response to a logical combination of (i) one or more voltage levels asserted at one or more first inputs, (ii) a state of one or more bond options connected to one or more second inputs and (iii) a state of one or more metal options connected to one or more third inputs; and

means for packaging said generating means comprising one or more pins dedicated to providing said one or more voltage levels to respective ones of said one or more first inputs.

21. The apparatus according to claim 1, wherein said apparatus can present any of said plurality of identification codes after packaging.

22. The apparatus according to claim 1, wherein said apparatus changes identification code in response to a change in said one or more voltage levels applied to said one or more pins.

23. The apparatus according to claim 1, wherein said package further comprises one or more pins dedicated to a test access port, at least one voltage supply pin and at least one ground pin.

24. The method according to claim 16, further comprising:

marking voltage level indications on said package after assembly to select a particular one of said plurality of identification codes for said die and package combination.

25. The method according to claim 16, further comprising:

changing voltage level indications provided to select different identification codes.

26. The apparatus according to claim 1, wherein:

each of said one or more metal options is configured to couple said respective one of said one or more third inputs to one of a pull-up device and a pull-down device.